In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A gateway apparatus for using in performing communication between wide area networks (WAN) to local area networks (LAN), comprising:

a plurality of input/output ports for connecting said WAN with said LAN;

a shared buffer device connected to the plurality of input/output ports for accessing packets, wherein a transporting path of said packets is selected from one of sending said packets from said WAN to said LAN and sending said packets from said LAN to said WAN;

a plurality of medium access control units corresponding to said input/output ports and electrically connected between said shared buffer device and said input/output ports for performing an accessing operation between said shared buffer device and said input/output ports;

a memory device electrically connected to said shared buffer device for storing said packets sent from said shared buffer device; and

a central processing unit electrically connected to said memory device and said medium access control units for processing said packets stored in said memory device, and organizing said medium access control units to change said input/output ports according to a required transporting path , thereby performing said communication between said LAN and said WAN.

2. (Original) The gateway apparatus according to claim 1, wherein said buffer device comprises:

a buffer for temporally storing said packets; and

a buffer manager electrically connected to said buffer for managing an accessing operation of said buffer device.

3. (Original) The gateway apparatus according to claim 1, wherein said memory device comprises :

a memory for storing said packets sent from said buffer device; and

a memory controller electrically connected to said memory for controlling an accessing operation of said memory.

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4. (Original) The gateway apparatus according to claim 3, wherein said memory is a dynamic random accessing memory (DRAM).

5. (Original) The gateway apparatus according to claim 3, further comprising:

an internal bus electrically connected to said memory controller for transporting said packets; and

a bus interface controller electrically connected between said buffer device and said internal bus for controlling a transporting operation in said internal bus so as to complete a packet transporting operation between said buffer device and said internal bus.

6. (Original) The gateway apparatus according to claim 1, wherein said buffer device, said medium access control units and said central processing unit are disposed in one identical chip.

7. (Original) The gateway apparatus according to claim 1, wherein said central processing unit is used for processing said packets stored in said memory device to achieve functions of a router and a firewall.

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